UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/046,304 | 01/16/2002 | Norihiko Moriwaki | 501.41034X00 | 2388 |

24956 7590 04/10/2006

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

| EXAMINER | |
|---|---|
| JAIN, RAJ K | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2616 | |

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/046,304 | MORIWAKI ET AL. | |
| | Examiner | Art Unit | |
| | Raj K. Jain | 2616 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/16/02* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

Figures 3, 4 and 26 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference "820" in Fig. 4 is not shown. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

Claim 1 objected to because of the following informalities: The words "accommodates" and "accommodated" are used which does not limit the scope of the claim and therefore suggest deleting or replacing the word to more clearly define the claimed the invention. Appropriate correction is required.

Claim 9 objected to because of the following informalities: In line 14 the phrase "the second line interface" is should be "crossbar switch". Appropriate correction is required.

Claim 12 objected to because of the following informalities: In line 6 of page 33 the phrase "in such a way" is used which does not limit the scope of the claim and therefore suggest revising the claim to more clearly define the claimed invention. Appropriate correction is required.

Claim 13 objected to because of the following informalities: In the last line replace the word "for" with "to". Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (Figs. 3, 4 and 26) in view of Yamazaki (US005600469A).

Regarding claim 1, Applicants admitted prior art discloses a packet communication system (see Figs. 26 which shows a packet communication system with ingress line cards and egress line cards and a crossbar switch for directing packets from the ingress card to the egress card.), comprising:

first line interface (see Fig. 3, which shows a line card 721 serving as the first line interface, see paras 0003-0004);

a second line interface that accommodates a line with a speed lower than that of a line accommodated by the first line interface (see Fig. 3, line interfaces 722, 723, 724 serving as second line interfaces accommodating line speeds lower than first line interface 721, see para 0004);

a crossbar switch (see Fig. 3, a crossbar switch 750 with plurality of input ports 731 and output ports 730.);

a scheduler that receives packet output requests from the first line interface and the second line interface periodically, and sends packet grants for the crossbar switch accordingly to the first and second line interfaces (see Fig. 26 and para 0003, The crossbar scheduler 705 receives a signal, referred to as a request, from an input queue. The request dictates the output channel or channels that will receive the queued packet. The scheduler arbitrates between competing requests and sends a signal, referred to as a grant, back to the input buffers that have been selected to deliver a packet. In

switches such as the one described in FIG. 26, each input queue provides requests to the scheduler, one at a time, and the scheduler arbitrates among the requests received from the input queues. As a grant is issued to a particular input channel to access a target output channel or channels, a new request is accessible by the scheduler in place of the granted request. A variety of arbitration techniques can be used with parallel input channels to provide an efficient throughput through a switch. One such technique is the round robin channel priority technique, under the rotating round-robin channel priority approach, every channel will periodically be designated as the highest priority, and therefore requests are processed between channels in round-robin priority order such that requests from channels with higher round-robin priority are granted access to output channels before requests from lower round-robin priority channels.).

Applicants admitted prior art fails to disclose a link capacity between the first line interface and the crossbar switch being larger than a link capacity between the second line interface and the crossbar switch.

Yamazaki discloses an optical network (see Figs. 1A and 1B) with plurality of line interface cards having different capacity output links from the interface cards to an exchange system which supports number of different subscriber needs (see FIG. 1A, which shows an optical network (ONU) connected to an exchange system, or central office, not shown, through single-mode fiber optic links 2 that support 156-Mb/s ATM cells in opposite directions. The ONU 1 comprises an optoelectric converter 3 connected to the end of the downward path of the links 2 to provide an amplification and optoelectrical conversion on the downlink optical ATM cells for coupling to a high speed

bus 6. To the bus 6 are connected a plurality of line interface cards 10, 20 and 30. Line interface cards 10, 20 and 30 are associated respectively with subscribers #1, #2 and #3 through drop lines 14, 24 and 34. Drop lines 14 are plastic fiber optic links supporting transfer rates of 50Mb/s associated with line interface card 10. Drop line 24 is a twisted pair of copper wires, supporting transfer rates of 64kb/s associated with line interface card 20. And Drop line 34 is a step index multimode fiber optic link, supporting transfer rates of 100Mb/s associated with line interface card 30, see col 2 line 10 – col 3 line 40.)

The use of various line capacities provides an efficient use of network bandwidth by allowing to size each interface line card with appropriate customer needs. Thus it would have been obvious at the time the invention was to modify Applicant's admitted prior art and with teachings Yamazaki so as to provide an more efficient use of network resources by allowing to resize each interface line card based on customer needs. Therefore the motivation for combining would have to been to improve efficiency of network resources.

Regarding claim 12, Applicants admitted prior art discloses a packet communication system (see Figs. 26 which shows a packet communication system with ingress line cards and egress line cards and a crossbar switch for directing packets from the ingress card to the egress card.), comprising:

-a plurality of first line interfaces (see Fig. 3, which shows a plurality of first line interfaces 723, 724, see paras 0003-0004);

a plurality of second line interfaces each having a speed equal to n times the speed of one of the plurality of first line interfaces (see Fig. 3, second line interfaces 721, and 722 accommodating line speeds n times that of first line interface 723, see para 0004); a crossbar switch (see Fig. 3, a crossbar switch 750 connected to the plurality of first and second line interfaces 721-724.);

a crossbar switch (see Fig. 3, a crossbar switch 750 connected to the plurality of line interfaces 721-724.);

a scheduler that receives packet output requests from the first line interface and the second line interface periodically, and sends packet grants for the crossbar switch accordingly to the first and second line interfaces (see Fig. 26 and para 0003, The crossbar scheduler 705 receives a signal, referred to as a request, from an input queue. The request dictates the output channel or channels that will receive the queued packet. The scheduler arbitrates between competing requests and sends a signal, referred to as a grant, back to the input buffers that have been selected to deliver a packet. In switches such as the one described in FIG. 26, each input queue provides requests to the scheduler, one at a time, and the scheduler arbitrates among the requests received from the input queues. As a grant is issued to a particular input channel to access a target output channel or channels, a new request is accessible by the scheduler in place of the granted request. A variety of arbitration techniques can be used with parallel input channels to provide an efficient throughput through a switch. One such technique is the round robin channel priority technique, under the rotating round-robin channel priority approach, every channel will periodically be designated as the highest

priority, and therefore requests are processed between channels in round-robin priority order such that requests from channels with higher round-robin priority are granted access to output channels before requests from lower round-robin priority channels.).

the scheduler controls the crossbar switch in such a way that the ingress of each one of the plurality of first line interfaces is connected to the egress the first line interfaces or the egress of one of the second line interfaces, and the ingress of each one of the second line interfaces is connected to the egresses of up to n ones first interfaces or the egress of another one of second line interfaces (Again see Fig. 26, the crossbar scheduler 705 is connected to plurality of line interface cards shown as solid line with double arrows from scheduler 705 to interface cards 1 thru n, and further the ingress 700 connects to the egress 704 of which inturn is connected to the scheduler 705 for requests and grants as appropriate.).

Applicants admitted prior art fails to disclose a varying link speeds between the first line interface and the crossbar switch and the second line interface and the crossbar switch.

Yamazaki discloses an optical network with plurality of line interface cards having different capacity output links from the interface cards to an exchange system which supports number of different subscriber needs (see FIG. 1A, which shows an optical network connected to an exchange system, or central office, not shown, through single-mode fiber optic links 2 that support 156-Mb/s ATM cells in opposite directions. The ONU 1 comprises an optoelectric converter 3 connected to the end of the downward path of the links 2 to provide an amplification and optoelectrical conversion on the

downlink optical ATM cells for coupling to a high speed bus 6. To the bus 6 are connected a plurality of line interface cards 10, 20 and 30. Line interface cards 10, 20 and 30 are associated respectively with subscribers #1, #2 and #3 through drop lines 14, 24 and 34. Drop lines 14 are plastic fiber optic links supporting transfer rates of 50Mb/s associated with line interface card 10. Drop line 24 is a twisted pair of copper wires, supporting transfer rates of 64kb/s associated with line interface card 20. And Drop line 34 is a step index multimode fiber optic link, supporting transfer rates of 100Mb/s associated with line interface card 30, see col 2 line 10 – col 3 line 40.)

The use of various line capacities provides an efficient use of network bandwidth by allowing to size each interface line card with appropriate customer needs. Thus it would have been obvious at the time the invention was to modify Applicant's admitted prior art and with teachings Yamazaki so as to provide an more efficient use of network resources by allowing to size each interface line card based on customer needs. Therefore the motivation for combining would have to been to improve efficiency of network resources.

Claims 2, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (Figs. 3, 4 and 26) as applied to claim 1 above in view of in view of Yamazaki (US005600469A) and further in view of Cloonan et al (US005550815A).

Regarding claim 2, Applicants admitted prior art (Fig. 26) discloses a conventional network switch with plurality of interface cards and a crossbar switch and

scheduler. Yamazaki discloses an optical network with plurality of line interface cards having different capacity output links from the interface cards.

Applicants admitted prior art and Yamazaki fail to disclose number of links between first line interface and the crossbar switch being greater than the number of links between the second line interface and the crossbar switch.

Cloonan discloses a packet data loss prevention method and apparatus in a growable packet switch (see Figs 9 and 14, col 5 lines 50-62, col 10 lines 46-67). Packet switch 100c is one configuration which has m input lines from first interface cards 106 connected to the switch 102c and n input lines to second interface cards 104A. The output of each input line interface card 106 is fanned-out and connected to m/n inputs of distribution network 102, where m/n is the concentration ratio of output packet modules 104A (second interface). Various combinations of m and n values (see col 8 lines 11-25) may be deployed based on the switch fabric handling capabilities and desired cell loss probabilities (ie. m<n, m=n or m>n). Thus for "m>n" the overall switch fabric hardware cost is increased, however, there is a significant "decrease in the cell loss probability" and therefore increase in the overall efficiency of the system. Thus the use of various link combinations between first and second interface cards allows control over reduction of cell loss probabilities with and system hardware cost. Thus one would be motivated at the time the invention was made to incorporate the teachings of Cloonan's link interface changes between first and second line cards within Applicants admitted prior art and Yamazaki so as to allow a reduction

of cell/packet loss probabilities while maintaining an acceptable level of system hardware cost.

Regarding claims 5 and 7, The switch described in FIG. 26 (Applicants admitted prior art), has input queue which provides requests to the scheduler 705, one at a time, and the scheduler arbitrates among the requests received from the input queues and issues a grant to access a target output channel. A variety of arbitration techniques are known in the art of schedulers which can be used with parallel input channels to provide an efficient throughput through a switch, thus resources may be scheduled sequentially or in parallel. Cloonan discloses an a crossbar switch (Fig. 9) with m input lines from first interface card 106 and n input lines to second interface card 104. The crossbar switch 102 and its controller 112 can receive upto N routing requests from the N arriving cells from either the first interface card or the second interface card (see col 8 lines 11-54) and respectively issue grants to sustain the requests received. Thus sequential arbitration amongst plurality of links from the same interface card that varies with number of input/output channels for each interface card correspondingly provides an equal number of grants being issued to sustain an acceptable access rate of packet transfer.

Thus one would be motivated at the time the invention was made to incorporate the an expandable packet switching network (of Cloonan) with varying number of links from first and second interface with Applicants admitted prior art and Yamazaki so as to sustain the required level of packet transfer between different interface cards with

different number of links and speeds to and from the crossbar switch while minimizing packet loss and improving transfer efficiency and cost.

Claims 3, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (Figs. 3, 4 and 26) as applied to claim 1 above in view of in view of Yamazaki (US005600469A) and further in view of Aybay (US006185221B1).

Applicants admitted prior art (Fig. 26) discloses a conventional network switch with plurality of interface cards and a crossbar switch and scheduler. Yamazaki discloses an optical network with plurality of line interface cards having different capacity output links from the interface cards.

Applicants admitted prior art and Yamazaki fail to disclose the scheduler performing specific task of requesting and/or granting more output packets requests and grants from one line interface as opposed to another line interface in the same cycle.

Aybay discloses a method and apparatus for scheduling data packets in a multipoint switch utilizing request buffers having multilevel request registers linked in parallel to a scheduler that arbitrates among requests based upon the location of the requests within the multilevel request buffers within an interface card and based upon a quality of service (QoS) priority assigned to the requests in order to maximize data packet transfer through the switch, while adhering to QoS requirements (see Fig. 5, col 3 lines 29 -61). There can be more than one request of the same QoS priority stored in a multilevel request buffer of a single channel, the location of a request stored within a multilevel request buffer, referred to as the request buffer priority, is used to award a grant among requests having the same QoS priority. Thus some channels and

therefore interface cards can have substantially more requests sent by the scheduler and thus inturn in equal number of grants being issued when the priority of the requests is same. A prioritization scheme of request and grant issuance provides an fair and efficient scheduling of packets within a swich. Therefore it would have been obvious at the time the invention was made to incorporate the teachings of Aybay within Applicants admitted prior art and Yamazaki so as to increase the efficiency of packet transfer between one or more interfaces cards while minimizing blocking by scheduling packets using a priority scheme. The motivation to combine would have been to increase the efficiency of packet transfer between one or more interfaces cards while minimizing blocking by scheduling packets using a priority scheme.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (Figs. 3, 4 and 26) as applied to claim 1 above in view of in view of Yamazaki (US005600469A) and further in view of Calvignac (US005251206A ).

Applicants admitted prior art (Fig. 26) discloses a conventional network switch with plurality of interface cards and a crossbar switch and scheduler. Yamazaki discloses an optical network with plurality of line interface cards having different capacity output links from the interface cards.

Applicants admitted prior art and Yamazaki fail to disclose the ratio of the maximum number of packet output requests received by the scheduler from the first line interface to maximum number of packet output requests received from the second line interface in the same cycle equals the ratio of the link capacity between the first

interface and the crossbar switch and the link capacity between the second line interface and the crossbar switch.

Calvignac discloses a hybrid switching system with varying traffics (see abstract, Figs. 1 and 4 and col 5 line 24- col 6 line ). Fig. 1 shows sharing the bandwidth between the hybrid switch 1 between packet and circuit traffic in a ratio determined by the needs of the circuit switched traffic or packet switched traffic. The sharing is adaptive since the proportion of circuit versus packet traffic can vary dynamically. Therefore a hybrid switching system provides an improved bandwidth utilization amongst different type of users having different capacity links. Thus, a link connected to an interface card having varying capacities (as taught Yamazaki) would proportionally have an equal number of requests/grants issued that is directly proportional in relation to the capacity of the link, in other words a link with a larger capacity to handle more data transfer would generate more request/grants to maintain optimum link performance than a link with having a much smaller capacity and therefore handles less data in proportion to the larger link. Therefore it would have been obvious at the time the invention was made to incorporate the teachings of Calvignac within Applicants 'admitted prior art' and Yamazaki so as to improve bandwidth utilization between the various link interfaces by having packet requests/grants that is directly proportional to their link interface capacities. The motivation to combine would have been to improve bandwidth utilization between the various link interfaces by having packet requests/grants that is directly proportional to their link interface capacities.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (Figs. 3, 4 and 26) as applied to claim 1 above in view of in view of Yamazaki (US005600469A) and further in view of Aybay (US006185221B1).

Applicants admitted prior art (Fig. 26) discloses a conventional network switch with plurality of interface cards and a crossbar switch and scheduler. Yamazaki discloses an optical network with plurality of line interface cards having different capacity output links from the interface cards.

Applicants admitted prior art and Yamazaki fail to disclose the scheduler performing specific task of requesting and/or granting more output packets requests and grants from one line interface as opposed to another line interface in the same cycle.

Aybay discloses a method and apparatus for scheduling data packets in a multipoint switch utilizing request buffers having multilevel request registers linked in parallel to a scheduler that arbitrates among requests based upon the location of the requests within the multilevel request buffers within an interface card and based upon a quality of service (QoS) priority assigned to the requests in order to maximize data packet transfer through the switch, while adhering to QoS requirements (see Fig. 5, col 3 lines 29 -61). There can be more than one request of the same QoS priority stored in a multilevel request buffer of a single channel, the location of a request stored within a multilevel request buffer, referred to as the request buffer priority, is used to award a grant among requests having the same QoS priority. Thus some channels and therefore interface cards can have substantially more requests sent by the scheduler and thus inturn in equal number of grants being issued when the priority of the requests

is the same. A prioritization scheme of request and grant issuance provides a fair and efficient scheduling of packets within a switch. Therefore it would have been obvious at the time the invention was made to incorporate the teachings of Aybay within Applicants admitted prior art and Yamazaki so as to increase the efficiency of packet transfer between one or more interfaces cards while minimizing blocking by scheduling packets using a priority scheme. Thus the motivation to combine would have been to increase the efficiency of packet transfer between one or more interfaces cards while minimizing blocking of scheduled packets.

Claims 8, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (Figs. 3, 4 and 26) in view of Cloonan et al (US005550815A).

Regarding claim 8, Applicants admitted prior art discloses a packet communication system (see Figs. 26 which shows a packet communication system with ingress line cards and egress line cards and a crossbar switch for directing packets from the ingress card to the egress card.), comprising:

-a plurality of first line interfaces (see Fig. 3, which shows a plurality of first line interfaces 723, 724, see paras 0003-0004);

a plurality of second line interfaces each having a speed equal to n times the speed of one of the plurality of first line interfaces (see Fig. 3, second line interfaces 721, and 722 accommodating line speeds n times that of first line interface 723, see para 0004);

a crossbar switch (see Fig. 3, a crossbar switch 750 connected to the plurality of line interfaces 721-724.);

a scheduler that receives packet output requests from the first line interface and the second line interface periodically, and sends packet grants for the crossbar switch accordingly to the first and second line interfaces (see Fig. 26 and para 0003, The crossbar scheduler 705 receives a signal, referred to as a request, from an input queue. The request dictates the output channel or channels that will receive the queued packet. The scheduler arbitrates between competing requests and sends a signal, referred to as a grant, back to the input buffers that have been selected to deliver a packet. In switches such as the one described in FIG. 26, each input queue provides requests to the scheduler, one at a time, and the scheduler arbitrates among the requests received from the input queues. As a grant is issued to a particular input channel to access a target output channel or channels, a new request is accessible by the scheduler in place of the granted request. A variety of arbitration techniques can be used with parallel input channels to provide an efficient throughput through a switch. One such technique is the round robin channel priority technique, under the rotating round-robin channel priority approach, every channel will periodically be designated as the highest priority, and therefore requests are processed between channels in round-robin priority order such that requests from channels with higher round-robin priority are granted access to output channels before requests from lower round-robin priority channels.).

the scheduler controls the crossbar switch in such a way that the ingress of each one of the plurality of first line interfaces is connected to the egress the first line

interfaces or the egress of one of the second line interfaces, and the ingress of each one of the second line interfaces is connected to the egresses of up to n ones first interfaces or the egress of another one of second line interfaces (Again see Fig. 26, the crossbar scheduler 705 is connected to plurality of line interface cards shown as solid line with double arrows from scheduler 705 to interface cards 1 thru n, and further the ingress 700 connects to the egress 704 of which inturn is connected to the scheduler 705 for requests and grants as appropriate.).

Applicants admitted prior art fails to disclose each of the plurality of second line interfaces connected to the crossbar switch by number of links equal to n times the number of links that provide connections between the plurality first line interfaces and the crossbar switch.

Cloonan discloses a packet data loss prevention method and apparatus in a growable packet switch (see Fig.3). Packet switch 100A has N input line interface cards 106A (first interface cards) that are connected to N lines carrying ATM cells. The output of each input line interface card 106A is fanned-out and connected to m/n inputs of distribution network 102A, where m/n is the concentration ratio of output packet modules 104A (second interface). The use of plurality of links between specific interface cards allows a reduction of cell loss probabilities with very little increase in system hardware cost. Thus it would have been obvious at the time the invention was made to incorporate the teachings of Cloonan's plurality of links in specific interface cards within Applicants admitted prior art so as to allow a reduction of cell/packet loss probabilities with very little increase in system hardware cost. Thus the

motivation for combining would have been to allow a reduction of cell/packet loss probabilities with very little increase in system hardware cost.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (Figs. 3, 4 and 26) as applied to claim 1 above in view of in view of Yamazaki (US005600469A) and further in view of Aybay (US006185221B1).

Applicants admitted prior art (Fig. 26) discloses a conventional network switch with plurality of interface cards and a crossbar switch and scheduler. Yamazaki discloses an optical network with plurality of line interface cards having different capacity output links from the interface cards.

Applicants admitted prior art and Yamazaki fail to disclose the scheduler performing specific task of requesting and/or granting more output packets requests and grants from one line interface as opposed to another line interface in the same cycle.

Aybay discloses a method and apparatus for scheduling data packets in a multipoint switch utilizing request buffers having multilevel request registers linked in parallel to a scheduler that arbitrates among requests based upon the location of the requests within the multilevel request buffers within an interface card and based upon a quality of service (QoS) priority assigned to the requests in order to maximize data packet transfer through the switch, while adhering to QoS requirements (see Fig. 5, col 3 lines 29 -61). There can be more than one request of the same QoS priority stored in a multilevel request buffer of a single channel, the location of a request stored

within a multilevel request buffer, referred to as the request buffer priority, is used to award a grant among requests having the same QoS priority. Thus some channels and therefore interface cards can have substantially more requests sent by the scheduler and thus inturn in equal number of grants being issued when the priority of the requests is same. A prioritization scheme of request and grant issuance provides an fair and efficient scheduling of packets within a swich. Therefore it would have been obvious at the time the invention was made to incorporate the teachings of Aybay within Applicants admitted prior art and Yamazaki so as to increase the efficiency of packet transfer between one or more interfaces cards while minimizing blocking by scheduling packets using a priority scheme.

Regarding claim 10, Applicants admitted prior art fails to disclose each of the plurality of second line interfaces connected to the crossbar switch by number of links equal to n times the number of links that provide connections between the plurality first line interfaces and the crossbar switch.

Cloonan discloses a packet data loss prevention method and apparatus in a growable packet switch. Packet switch 100B (Fig. 6) has m/n input links from the first interface cards 106B to a crossbar switch 102B, and n-1 number of input links to the second interfaces 104A, where m and n are arbitrary values depending upon the crossbar switch configuration (see col 8 lines 50-65). The output of each input line interface card 106A is fanned-out and connected to m/n inputs of distribution network 102B, where m/n is the concentration ratio of output packet modules 104A (second interface). The use of plurality of links between specific interface cards allows a

reduction of cell loss probabilities with very little increase in system hardware cost. Thus it would have been obvious at the time the invention was made to incorporate the teachings of Cloonan's plurality of links in specific interface cards within Applicants admitted prior art so as to allow a reduction of cell/packet loss probabilities with very little increase in system hardware cost.

Regarding claim 11, Applicants admitted prior art (Fig. 3) discloses a first line interface having transmitting driver 730 at the ingress connected to a receiver 731 at the egress in a single link.

Applicants prior art fails to show multiple transmitters and receivers when more than one link is entertained within a given interface.

Cloonan discloses a packet data loss prevention method and apparatus in a growable packet switch. Packet switch 100B (Fig. 6) has m/n input links from the first interface cards 106B to a crossbar switch 102B, and n-1 number of input links to the second interfaces 104A, where m and n are arbitrary values depending upon the crossbar switch configuration (see col 8 lines 50-65). Furthermore, each link within the interface card connecting to the crossbar switch would have an appropriate output port for transmitting packets (driver) and input port (receiver driver) for receiving of packets, and thus an interface card having two or more links connected with the crossbar switch would have appropriately two transmitting drivers and two receiving drivers that can accommodate both the links independently. The use of plurality of links between specific interface cards allows a reduction of cell loss probabilities with very little

increase in system hardware cost. Thus it would have been obvious at the time the invention was made to incorporate the teachings of Cloonan's plurality of links in specific interface cards within Applicants admitted prior art so as to allow a reduction of cell/packet loss probabilities with very little increase in system hardware cost.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Raj Jain whose telephone number is 571-272-3145. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

R. Jain

RJ
March 31, 2006